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Title:

DRAM ACCESS TRANSISTOR AND METHOD OF FORMATION

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DRAM ACCESS TRANSISTOR AND METHOD OF FORMATION

FIELD OF THE INVENTION

[0001]   The present invention relates to dynamic random access memory (DRAM) cells and, in particular, to a novel process for their formation.

BACKGROUND OF THE INVENTION

[0002]   A dynamic random access memory cell typically comprises a charge storage capacitor (or cell capacitor) coupled to an access device, such as a Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET). The MOSFET functions to apply or remove charge on the capacitor, thus affecting a logical state defined by the stored charge. The amount of charge stored on the capacitor is determined by the electrode (or storage node) area and the interelectrode spacing. The conditions of DRAM operation such as operating voltage, leakage rate and refresh rate, will generally mandate that a certain minimum charge be stored by the capacitor.

[0003]   In the continuing trend to higher memory capacity, the packing of storage cells must increase, yet each must maintain required capacitance levels. This is a crucial demand of DRAM fabrication technologies. Recently, attempts to increase the packing density of cell capacitors and/or to simultaneously reduce the transistor size have been made but with limited results. For example, one approach is reducing the length of a transistor gate electrode formed atop a substrate and a source/drain region, to increase therefore the integration density. Unfortunately, reduction of the threshold voltage and/or the so-called short channel effect such as the punch-through phenomenon are likely to appear. A well-known scaling method is effective to improve the above-mentioned disadvantages. However, this approach increases the substrate doping density and requires reduction of the

supply voltage, which in turn leads to reduction of the margin concerning the electric noise and fluctuations in the threshold voltage. Higher channel doping causes degradation in retention time due to high electric field at the storage node junction.

[0004]   Accordingly, there is a need for an improved method of forming MOS semiconductor devices, which permits achieving an increased integration of semiconductor circuitry as well as preventing the occurrence of the short-channel effect without adding more dopants into the channel.

SUMMARY OF THE INVENTION

[0005]   An embodiment of the present invention provides a method of forming memory devices, such as DRAM access transistors, having self-aligned recessed gate structures. A plurality of insulating columns are defined in an insulating layer formed over the semiconductor substrate subsequent to which a thin sacrificial oxide layer is formed over exposed regions of the semiconductor substrate. A dielectric material is then provided on sidewalls of each column and over portions of the sacrificial oxide layer. A first etch is conducted to form a first set of trenches of a first width within the semiconductor substrate. As a result of the first etch, the thin sacrificial oxide layer is completely removed, but the dielectric material is only partially removed forming dielectric residue on the sidewalls of the columns. A second etch is conducted to remove the dielectric residue remaining on the sidewalls of the columns and to form a second set of trenches of a second width which is greater than the first width of the first set of trenches.

[0006]   Another embodiment of the present invention provides a self-aligned recessed gate structure for DRAM access transistors. The self-aligned recessed gate structure comprises a first recessed gate region located below a surface of a semiconductor substrate and having a width of about 35 nm to about 75 nm, more preferably of about 60 nm. The self-aligned recessed gate structure also comprises

a second gate region extending above the surface of said semiconductor substrate by about 20 nm to about 800 nm. The second gate region has a width of about 50 nm to about 100 nm, more preferably of about 80 nm. Insulating spacers are located on sidewalls of the second gate region but not on sidewalls of the first recessed gate region.

[0007]   These and other advantages and features of the present invention will be more apparent from the detailed description and the accompanying drawings, which illustrate exemplary embodiments of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008]   Figure 1 illustrates a schematic cross-sectional view of a portion of a semiconductor device on which a DRAM access transistor will be formed according to a method of the present invention.

[0009]   Figure 2 illustrates a cross-sectional view of the Figure 1 device at a stage of processing subsequent to that shown in Figure 1.

[0010]   Figure 3 illustrates a cross-sectional view of the Figure 1 device at a stage of processing subsequent to that shown in Figure 2.

[0011]   Figure 4 illustrates a cross-sectional view of the Figure 1 device at a stage of processing subsequent to that shown in Figure 3.

[0012]   Figure 5 illustrates a cross-sectional view of the Figure 1 device at a stage of processing subsequent to that shown in Figure 4.

[0013]   Figure 5a illustrates a cross-sectional view of the Figure 5 device taken along line 5-5'.

[0014]   Figure 6 illustrates a cross-sectional view of the Figure 1 device at a stage of processing subsequent to that shown in Figure 5.

[0015]   Figure 6a illustrates a cross-sectional view of the Figure 6 device taken along line 6-6'.

[0016]   Figure 7 illustrates a cross-sectional view of the Figure 1 device at a stage of processing subsequent to that shown in Figure 6.

[0017]   Figure 8 illustrates a cross-sectional view of the Figure 1 device at a stage of processing subsequent to that shown in Figure 7.

[0018]   Figure 9 illustrates a cross-sectional view of the Figure 1 device at a stage of processing subsequent to that shown in Figure 8.

[0019]   Figure 10 illustrates a cross-sectional view of the Figure 1 device at a stage of processing subsequent to that shown in Figure 9.

[0020]   Figure 11 illustrates a cross-sectional view of the Figure 1 device at a stage of processing subsequent to that shown in Figure 10.

[0021]   Figure 12 illustrates a cross-sectional view of the Figure 1 device at a stage of processing subsequent to that shown in Figure 11.

[0022]   Figure 13 illustrates a cross-sectional view of the Figure 1 device at a stage of processing subsequent to that shown in Figure 12.

[0023]   Figure 14 is an illustration of a computer system having a DRAM access transistor formed according to a method of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0024]   In the following detailed description, reference is made to various specific exemplary embodiments in which the invention may be practiced. These embodiments are described with sufficient detail to enable those skilled in the art to practice the invention, and it is to be understood that other embodiments may be employed, and that structural, logical, and electrical changes may be made.

[0025]   The terms "wafer" or "substrate" used in the following description may include any semiconductor-based structure that has a semiconductor surface. Wafer and structure must be understood to include silicon, silicon-on insulator (SOI), silicon-on sapphire (SOS), doped and undoped semiconductors, epitaxial layers of silicon supported by a base semiconductor foundation, and other semiconductor structures. The semiconductor need not be silicon-based. The semiconductor could be silicon-germanium, germanium, or gallium arsenide.

[0026]   Referring now to the drawings, where like elements are designated by like reference numerals, Figures 1-13 illustrate a method of forming a DRAM memory device 100 (Figure 13) having access transistors formed according to exemplary embodiments of the present invention. Figure 1 illustrates a semiconductor substrate 10 within which shallow trenches isolation (STI) regions 20 have been formed by conventional methods. In one exemplary embodiment, to obtain the shallow trenches isolation regions 20, the substrate 10 is first etched to a depth of about 100 nm to about 1,000 nm, preferably of about 300 nm. Subsequent to the formation of the shallow trenches, the trenches are filled with an isolation dielectric, for example, a high density plasma (HDP) oxide, a material which has a high ability to effectively fill narrow trenches. Alternatively, an insulating layer formed of an oxide or of silicon nitride, for example, may be formed on the trench sidewalls, prior to filling the trenches with the isolation dielectric, to aid in smoothing out the corners in the bottom of the trenches and to reduce the amount of stress in the dielectric used to later fill in the trenches.

[0027]   Figure 1 also illustrates an insulating layer 14 formed over the semiconductor substrate 10 according to conventional semiconductor processing techniques. Insulating layer 14 may comprise a silicon oxide such as a TEOS oxide or a nitride such as silicon nitride (Si_3N_4), for example. The insulating layer 14 is formed over the substrate 10 to a thickness of about 10 nm to about 1,000 nm, more preferably of about 200 nm. Although reference to the insulating layer 14 will be made in this application as to the TEOS oxide layer 14, it must be understood that the insulating layer 14 may be also formed of silicon nitride, for example, or other insulating materials, and thus the invention is not limited to the use of TEOS oxide. The TEOS oxide layer 14 may be formed by known deposition processes such as chemical vapor deposition (CVD) or low temperature deposition by electron cyclotron resonance plasma enhanced CVD, among others.

[0028]   Next, the TEOS oxide layer 14 is patterned using a photoresist layer 15 (Figure 1) formed over the TEOS oxide layer 14 to a thickness of about 100 nm to about 1,000 nm. The photoresist layer 15 is patterned with a mask (not shown) and the TEOS oxide layer 14 is anisotropically etched through the patterned photoresist to obtain a plurality of TEOS oxide columns 18 or lines (Figure 2) having a width W of about 50 nm to about 100 nm, more preferably of about 80 nm, and a height H of about 20 nm to about 800 nm, more preferably of about 200 nm. As shown in Figure 2, the TEOS oxide columns 18 are spaced apart from each other by a distance D (illustratively about equal to the width W) of about 50 nm to about 100 nm, more preferably of about 80 nm. As described in more detail below, the distance D represents the width of the portions of the self-aligned recessed gate structures located above the surface of the substrate 10 and formed according to embodiments of the present invention. The TEOS oxide columns 18 also define regions A adjacent and above surface 11 of the semiconductor substrate 10 and regions B adjacent and above the dielectric material of the STI regions 20, as shown in Figure 2.

[0029]   The photoresist layer 15 is removed by conventional techniques, such as oxygen plasma, for example, or by flooding the substrate 10 with UV irradiation to degrade the photoresist and obtain the structure of Figure 2.

[0030]   Reference is now made to Figure 3. Subsequent to the formation of the TEOS oxide columns 18, a thin sacrificial oxide layer 22 with a thickness of about 3 nm to about 20 nm, more preferably of about 5 nm, is thermally grown over exposed surfaces 19 (Figure 2) of the semiconductor substrate 10 corresponding to regions A but not corresponding to regions B, as illustrated in Figure 3. Since regions B are located over the field isolation oxide in regions 20, the oxide grown in the regions B is undetectable. As described in more detail below, the sacrificial oxide layer 22 will be employed as an etch stop layer during a poly spacer etch. Subsequent to the formation of the sacrificial oxide layer 22, a doped or undoped polysilicon layer 24 is formed over the TEOS oxide columns 18, the thin sacrificial oxide layer 22 and the dielectric material of the STI regions 20, as shown in Figure 3. The polysilicon layer 24 is formed to a thickness of about 1/4 to 1/3 of the width W or distance D (Figure 2), by a deposition technique, for example CVD or LPCVD procedures, at a temperature of about 300°C to about 600°C.

[0031]   The polysilicon layer 24 formed over the TEOS oxide columns 18, over the thin sacrificial oxide layer 22 and over the dielectric material of the STI regions 20 is then partially etched with a first etchant, such as a selective etchant with HBr based chemistry, for example, that stops on the sacrificial oxide layer 22 and on the dielectric material of the STI regions 20 and forms polysilicon spacers 25, 25a, as shown in Figure 4. The height of the polysilicon spacers 25, 25a is adjustable by overetching, depending on the desired depth of the recessed gate. For example, in one particular embodiment, the height of the polysilicon spacers 25, 25a is of about 50 nm to about 500 nm, more preferably of about 100 nm.

[0032]   Subsequent to the formation of the polysilicon spacers 25, 25a of Figure 4, the semiconductor substrate 10 is etched by a directional etching process with a second etchant having a high selectivity to oxide in a HBr ambient, for example, to a depth λ_1 (Figure 5) of about 100 nm to about 500 nm, more preferably of about 100 nm to about 150 nm, to obtain first transistor trenches or grooves 28 (Figures 5; 5a) where a first set of recessed self-aligned gate structures of the DRAM memory device 100 (Figure 12) will be later formed as it will be described in detail below. At the end of the formation of the first transistor trenches 28, the polysilicon spacers 25 are almost totally consumed, with polysilicon residues 26 remaining adjacent the first transistor trenches 28, as shown in Figure 5. The sacrificial oxide layer 22 under spacers 25 is not consumed to protect the silicon surface from pitting caused by the silicon-etch process. The first transistor grooves 28 are formed to a width W_1 (Figure 5) which is about 1/2 of the distance D of Figure 2.

[0033]   During the selective etch for the formation of the first transistor trenches 28, the dielectric material of the STI regions 20 is also etched to a depth δ (Figure 5) of about 1 nm to about 10 nm, more preferably of about 5 nm. This etching of the dielectric material depends on etch selectivity of polysilicon etch with respect to oxide. The selective etching produces polysilicon residues 26a (the same as residues 26) and STI recesses 29 (Figure 5) where a second set of recessed self-aligned gate structures of the DRAM memory device 100 (Figure 12) will be later formed as it will be described in detail below.

[0034]   Subsequent to the formation of the first transistor trenches 28 (Figures 5; 5a) and of the STI recesses 29 (Figure 5), a third etch, for example an isotropic etch or a wet etch such as a TMAH etch, is next conducted to remove polysilicon residues 26, 26a remaining adjacent the first transistor trenches 28 and the STI recesses 29, respectively, and to obtain the structure of Figure 6. As a result of the isotropic or wet etch, second transistor trenches or grooves 30

(Figures 6; 6a) are also formed to a width W_2 which is greater than the width W_1 of the first transistor trenches 28, that is to a width W_2 which is up to 3/4 the distance D of Figure 2. Second transistor grooves 30 are also formed to a depth λ_2 (Figure 6), which is greater than the depth λ_1 of the first transistor grooves, that is to a depth λ_2 of about 200 nm to about 700 nm, more preferably of about 250 nm to about 300 nm.

[0035]   An optional cleaning step of all exposed surfaces of the semiconductor substrate 10 of Figure 6 may be conducted at this step of processing. Alternatively, another sacrificial silicon oxide layer may be grown over the exposed surfaces of the semiconductor substrate 10 of Figure 6 and then stripped by conventional methods to ensure removal of any existent impurities, particulates and/or residue from the exposed surfaces, and to also smooth the silicon surface in the groove 30.

[0036]   Subsequent to the formation of the second transistor trenches 30 and to the optional cleaning step, a thin gate oxide layer 32 is selectively formed on the sidewalls and bottoms of the second transistor trenches 30 and on the adjacent exposed surfaces of the semiconductor substrate 10 corresponding to regions A but not over the recesses 29 corresponding to regions B, as shown in Figure 7. The thin gate oxide layer 32 may be thermally grown in an oxygen ambient, at a temperature between about 600°C to about 1,000°C and to a thickness of about 3 nm to about 10 nm.

[0037]   A polysilicon material 33 (Figure 7) is then formed within both regions A, B as well as inside the second transistor trenches 30 and the STI recesses 29 of the substrate 10. The polysilicon material 33 may be may be doped n+ or p+ and may be blanket deposited over the structure of Figure 7, via LPCVD procedures at a temperature of about 300°C to about 600°C, for example, to completely fill regions A and B. Once regions A and B are completely filled, the polysilicon material 33 is subjected to a mild isotropic poly etch to etch back parts

of the polysilicon from regions A and B and to form polysilicon gate layers 35 corresponding to regions A and to second transistor trenches 30, and polysilicon gate layers 36 corresponding to regions B and to STI recesses 29, as shown in Figure 8. The polysilicon gate layers 35, 36 extend above the surface 11 of the semiconductor substrate 10 by a distance H_1 (Figure 8) of about 5 nm to about 100 nm, more preferably by about 25 nm. It must be noted that the height H_1 of the polysilicon gate layers 35, 36 must be smaller than the height H of the TEOS oxide columns 18, to allow the formation of the remaining metal-clad gate stack structures, as described in detail below.

[0038]   Referring still to Figure 8, a barrier layer 37 of about 5 nm to about 40 nm is next formed over the polysilicon gate layers 35, 36. The barrier layer 37 may be formed of tungsten nitride (WNx), titanium nitride (TiN) or titanium-rich TiN material, among others. Alternatively, the barrier layer 37 may be a transition metal boride layer such as zirconium boride (ZrBx), titanium boride (TiBx), hafnium boride (HfBx) or tantalum boride (TaBx). Such materials exhibit good adhesion characteristics to silicon and, due to the low resistivities of about 5-150 microOhms-cm of the transition metal borides, the total height of the gate stack can be decreased.

[0039]   Subsequent to the formation of the barrier layer 37, a conductive material 39 (Figure 8) is formed, by blanket deposition for example, over the barrier layer 37 and over the TEOS oxide columns 18, to completely cover the structure of Figure 8. The conductive material 39 and the barrier layer 37 are then subjected to a CMP process, for example, and subsequently to an etching process to remove portions of the conductive material 39 and of the barrier layer 37 from the top of the TEOS oxide columns 18 and from in between the TEOS oxide columns 18, to form highly conductive metal stacks 45, as shown in Figure 9. Each of the highly conductive stacks of Figure 9 includes a patterned barrier layer 38 and a conductive layer 40. The conductive layer 40 can comprise a material

such as titanium (Ti) or titanium nitride (TiN), among others, or simply, it can be formed by a silicide process such as cobalt silicide (CoSi), titanium silicide (TiSi), molybdenum silicide (MoSi) or nickel silicide (NiSi), among others. As known in the art, TiSi and CoSi do not adhere well to gate dielectric materials and, as a consequence, they may lift from the gate dielectric materials; however, NiSi and MoSi are known to adhere well to gate dielectric materials and they are fully silicided when formed on an existing thin polysilicon film.

[0040]   An insulating cap material of about 50 nm to about 100 nm is next deposited over substrate 10 to completely fill regions A and B of Figure 8 and the substrate top surface is planarized so that cap regions 55 (Figure 9) are formed over the highly conductive metal stacks 45. The cap material may be formed of silicon dielectrics such as silicon nitride or silicon oxide, but TEOS, SOG (spin on glass) or carbides may be used also. The cap material may be also formed of an etch-stop insulating material.

[0041]   Although the embodiments detailed above have been described with reference to the formation of a barrier layer, such as the transition metal boride layer 37, and of the conductive layer 40 formed over the transition metal boride layer 37 to form highly conductive metal stacks 45, it must be understood that the invention is not limited to these embodiments. Accordingly, the present invention also contemplates the formation of other gate structures in lieu of the highly conductive metal stacks 45. For example, and according to another embodiment of the present invention, a thin film of a transition metal such as titanium (Ti) or titanium nitride (TiN) having a thickness of less than 30 nm can be deposited over the polysilicon gate layers 35, 36 by a PVD or CVD process. Optionally, the titanium or titanium nitride film can be further exposed to a gas containing a dopant element such as boron, for example. If boron is employed, the wafer is placed in a rapid thermal process (RTP) chamber and a flow of B_2H_6 or BF_3 gas diluted with hydrogen (H_2), nitrogen (N_2) and/or argon (Ar) gas is provided in

the vicinity of the titanium or titanium nitride film to form the transition metal boride film.

[0042]   In yet another embodiment, a thin film of a transition metal such as titanium (Ti) is deposited over the polysilicon gate layers 35, 36 and then the polysilicon gate layers and the transition metal film are subsequently implanted with a dopant such as boron. Accordingly, a doped polysilicon and the transition metal layer 37 can be formed by a single boron implant.

[0043]   Alternatively, a layer of metal capable of forming a silicide (not shown) such as cobalt, nickel, molybdenum, titanium or tungsten, for example, may be deposited over the polysilicon gate layers 35, 36 to a thickness of about 20 nm to about 50 nm. For deposition, sputtering by RF or DC may be employed but other similar methods such as CVD may be used. Subsequent to the deposition of the metal capable of forming a silicide, substrate 10 undergoes a rapid thermal anneal (RTA), typically for about 10 to 60 seconds, using a nitrogen ambient, at about 600°C to about 850°C so that the metal in direct contact with the polysilicon gate layers 35, 36 is converted to its silicide. The silicide regions form conductive regions on top of the polysilicon gate layers 35, 36. Preferably, the refractory metal has low resistance and low resistivity as a silicide. However, the refractory metal silicide may comprise any refractory metal, including but not limiting to titanium, cobalt, tungsten, tantalum, molybdenum, nickel and platinum. If a silicide is employed, barrier layer 37 as described above may be also optionally employed. The barrier layer 37 may be also omitted to simplify the process steps. In any event, care must be taken later on during the processing to prevent tungsten or silicide materials from being oxidized during the source/drain oxidation.

[0044]   Reference is now made to Figure 10. Subsequent to the formation of the highly conductive metal stacks 45 and of the cap regions 55 (Figure 9), the TEOS oxide columns 18 are removed by etching, for example, so that the

formation of self-aligned recessed gate stacks 90, 190 (Figure 10) of DRAM memory device 100 is completed. Although the following processing steps for the completion of the self-aligned recessed gate stacks 90, 190 will refer to and illustrate the highly conductive metal stacks 45 comprising conductive layer 40 formed over the patterned barrier layer 38 and polysilicon gates layers 35, 36, it must be understood that the present invention is not limited to this embodiment, and other embodiments such as the formation of gate stacks comprising a dielectric material (for example, a high-k dielectric material) formed over the polysilicon gates, for example, are also contemplated. Additionally, gate stacks comprising non-silicide materials such as TiN, WN, Ta, TaN or Nb, among others, which may be employed as direct gate materials on gate dielectrics, are also contemplated by the present invention, and it must be understood that the above-described embodiments are only exemplary and the invention is not limited to them.

[0045]   At this point self-aligned recessed gate stacks 90 (Figure 10) (each having gate oxide layer 32, polysilicon gate layer 35, highly conductive metal stack 45 and nitride cap 55) and self-aligned recessed gate stacks 190 (Figure 10) (each having polysilicon gate layers 36, highly conductive metal stack 45 and nitride cap 55) have been formed. The self-aligned recessed gate stacks 90, 190 may now be used in a conventional implant process where the gate structures are used as masks for the dopant implantation of source and drain regions as further described below.

[0046]   At this point, processing steps for transistor formation proceed according to conventional semiconductor processing techniques. The next step in the flow process is the growth of a selective oxide 94 (Figure 11) on the exposed surfaces of the semiconductor substrate 10 obtained as a result of the removal of the TEOS oxide columns 18 (Figure 9), as well as on the polysilicon sidewalls of the gate stacks 90, 190. The selective oxide 94 may be thermally grown in an oxygen and hydrogen ambient, at a temperature between about 600°C to about 1,000°C and to a thickness of about 3 nm to about 8 nm. Subsequent to the

formation of the selective oxide 94, a layer 95 of spacer dielectric material, such as nitride material for example, is formed over the gate stacks 90, 190 and the selective oxide 94, as shown in Figure 11.

[0047]   The self-aligned recessed gate stacks 90, 190 protected by layer 95 of nitride material and by the selective oxide 94 can now undergo conventional processing steps for the formation of source and drain regions 92, 96 and of lightly doped drain (LDD) regions 96a, as shown in Figure 12. For this, doping through layer 95 and the selective oxide 94 is conducted to form the source and drain regions 92, 96 and the lightly doped drain (LDD) regions 96a, subsequently to which layer 95 and selective oxide 94 are etched back to form nitride spacers 95a, also illustrated in Figure 12. Alternatively, the layer 95 of nitride material and the selective oxide 94 are first etched back to form nitride spacers 95a, and then the resulting structure is subjected to doping for the formation of the source and drain regions 92, 96 and the lightly doped drain (LDD) regions 96a.

[0048]   Subsequent to the formation of the source and drain regions 92, 96 and the lightly doped drain (LDD) regions 96a of Figure 12, contact openings for conductors 117 and/or capacitors 107 into semiconductor substrate 10 through an oxide layer 110 such as BPSG, for example, are also formed to produce a semiconductor device such as the DRAM memory device 100, all illustrated in Figure 13. Although, for simplicity, Figure 13 illustrates the formation of bit line 118 over the capacitor structures 107, it must be understood that this embodiment is only exemplary and the invention also contemplates the formation of a bit line under capacitor (or capacitor over bit line (COB)). In fact, an embodiment with a COB is desirable as it would decrease the length of the plug to silicon which, in turn, would decrease the parasitic capacity of the bit line.

[0049]   The self-aligned recessed gate stacks 90, 190 (Figures 10-13) and associated transistors formed in accordance with embodiments of the present invention could be used in any integrated circuit structure. In one example, they

can be used in a processor-based system 400 which includes a memory circuit 448, for example the DRAM memory device 100, as illustrated in Figure 14. A processor system, such as a computer system, generally comprises a central processing unit (CPU) 444, such as a microprocessor, a digital signal processor, or other programmable digital logic devices, which communicates with an input/output (I/O) device 446 over a bus 452. The memory 448 communicates with the system over bus 452.

[0050]   Although the embodiments of the present invention have been described above with reference to the formation of self-aligned recessed gate stacks 90, 190 comprising specific materials, such as the polysilicon material for the formation of layers 35, 36 for example, it must be understood that the present invention is not limited to these specific examples. Accordingly, the present application has applicability to other gate metals or materials known in the art, or combination of such metals and materials, for the formation of the self-aligned recessed gate stacks 90, 190 of the present invention.

[0051]   In addition, although the embodiments of the present invention have been described above with reference to the formation of polysilicon spacers, such as the polysilicon spacers 25, 25a, over a thin oxide layer, such as the thin sacrificial oxide layer 22, and over TEOS oxide columns, such as TEOS oxide columns 18, it must be understood that the present invention is not limited to these three specific materials. Accordingly, the present application has applicability to other materials, or combination of such materials, for the formation of the spacers, of the oxide layer and of the columns used for the formation of the self-aligned recessed gate stacks 90, 190. For example, the present invention also contemplates using a high-k dielectric material, HfO_2, or Al_2O_3/ZrO_2, among others, in addition to the conventional oxide and nitride materials. Thus, the polysilicon/oxide/TEOS oxide combination (corresponding to the polysilicon

spacers/thin oxide layer/TEOS oxide columns) is only one exemplary embodiment of the present invention.

[0052]   The above description and drawings are only to be considered illustrative of exemplary embodiments which achieve the features and advantages of the present invention. Modification and substitutions to specific process conditions and structures can be made without departing from the spirit and scope of the present invention. Accordingly, the invention is not to be considered as being limited by the foregoing description and drawings, but is only limited by the scope of the appended claims.